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ARCHITECTURE EXPLORATION OF FPGA BASED ACCELERATORS FOR BIOINFORMATICS APPLICATIONS by B. SHARAT CHANDRA VARMA Amar Nath and Shashi Khosla School of Information Technology

ARCHITECTURE EXPLORATION OF FPGA BASED ACCELERATORS FOR

This paper presents a hardware module design for the forward Binary Discrete Cosine Transform (BinDCT) and its implementation on a field programmable gate array device.

(PDF) Efficient BinDCT hardware architecture exploration

The book also explains how the respective HEBs are designed and how hardware implementation of the application is done using these HEBs. It shows that significant speedups can be achieved over pure software implementations by using such FPGA-based accelerators.

Architecture Exploration of FPGA Based Accelerators for

Extra info for Architecture Exploration of FPGA Based Accelerators for BioInformatics Applications Sample text For example assembly of human genome using PASHA software took around 21 h on a 8-core workstation with 72 GB memory [56].

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Architecture Exploration Of Fpga Based Accelerators For

Visualization Support for FPGA Architecture Exploration by K. Nasartschuk, K. B. Kent and R. Herpers TR 11-213, December 1, 2011 Faculty of Computer Science

Visualization Support for FPGA Architecture Exploration

FPRESSO: Enabling Express Transistor-Level Exploration of FPGA Architectures Grace Zgheib grace.zgheib@epi-,.ch Manana Lortkipanidze manana.lortkipanidze@epi-,.ch Muhsen Owaida mohsen.ewaida@epi-,.ch

FPRESSO: Enabling Express Transistor-Level Exploration of

propose an FPGA-based accelerator architecture. We develop analytical feasibility and performance estimation models that take into account various design and platform parameters. Consequently, we develop a design space exploration algorithm using which, we obtain the implementation with the highest performance for a given target FPGA platform.

Design Space Exploration of FPGA-Based Deep Convolutional

throughput. Mars exploration rovers currently use Xilinx-Space-grade FPGA devices for image processing, pyrotechnic operation control and obstacle avoidance. The hardware resource consumption for the architecture has been synthesized considering Xilinx Virtex7 FPGA as the target device.

FPGA Accelerator Architecture for Q-learning and its

BASICS OF FIELD PROGRAMMABLE GATE ARRAYS WaqarWaqar Hussain Hussain

firstname.lastname@tut.fi Department of Computer Systems Tampere University Tampere University of Technology of Technology Lecture Contents 1. Why there was a need for FPGA ? 2. What is the Scope of FPGA usability ? 3. How to Implement a Digital System ? 4. FPGA Architecture 5.

BASICS OF FIELD PROGRAMMABLE GATE ARRAYS

FIELD PROGRAMMABLE GATE ARRAYS (FPGA) FPGA provide the next generation in the programmable logic devices. The word Field in the name refers to the ability of the gate arrays to be programmed for a specific

FIELD PROGRAMMABLE GATE ARRAYS (FPGA)

PDF | An innovative 3D physical design exploration methodology for Tree-based FPGA architecture is presented in this paper.

(PDF) Physical Design Exploration of 3D Tree-based FPGA

Architecture of FPGAs and CPLDs: A Tutorial Stephen Brown and Jonathan Rose Department of Electrical and Computer Engineering University of Toronto email: brown | jayar@eecg.toronto.edu Abstract This paper provides a tutorial survey of architectures of commercially available high-capacity field-programmable devices (FPDs).

Architecture of FPGAs and CPLDs: A Tutorial

The architecture based on the S.2, S.2, S.2 and S.3 implementation solutions for stages 1, 2, 3 and 4 is also considered as an architectural exploration starting point. In Table 3 , this architecture is called "medium shared solution".

Efficient BinDCT hardware architecture exploration and

FPGA Routing Architecture: Segmentation and Buffering to Optimize Speed and Density Vaughn Betz and Jonathan Rose Department of Electrical and Computer Engineering, University of Toronto

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